WHAT IS CLAIMED IS:

1. A resistance measurement circuit comprising:

a plurality of current sources;

a plurality of resistor strings, wherein each resistor string is coupled in series with a respective one of the current sources and comprises a plurality of nodes with different resistances relative to a reference node, and wherein each node in each resistor string has a different resistance relative to the reference node than corresponding nodes in the other resistor strings; and

a comparator having a first comparison input coupled to a reference voltage and a second comparison input selectively coupled to the plurality of nodes in each resistor string.

2. The resistance measurement circuit of claim 1 wherein:

the plurality of resistor strings comprises a sequence of the resistor strings; and

each set of the corresponding nodes in the plurality of resistor strings have progressively varying resistances within the sequence.

3. The resistance measurement circuit of claim 2 wherein:

each node in each resistor string has a smaller resistance relative to the reference node than the corresponding node in the next preceding resistor string in the sequence and a larger resistance relative to the reference node than the corresponding node in the next succeeding resistor string in the sequence.

4. The resistance measurement circuit of claim 2 wherein:

each resistor string comprises a plurality of resistors coupled in series with one another; and

each resistor string further comprises a least significant one of the resistors, which is coupled to the reference node, and a different number of parallel resistors coupled in parallel with the least significant resistor than are coupled in parallel with the least significant resistors in the other resistor strings.

5. The resistance measurement circuit of claim 2 wherein:

the plurality of resistor strings comprises m+1 resistor strings, which can be indexed in the sequence by a variable i, for i = 0 to m+1, where m is an integer variable;

each resistor string i comprises a plurality of resistors coupled in series with one another, including at least one least significant resistor that is connected to the reference node;

wherein the at least one least significant resistor in resistor string i comprises 2^i resistors coupled in parallel with one another.

6. The resistance measurement circuit of claim 5 wherein each resistor in each resistor string has a unit resistance.

7. The resistance measurement circuit of claim 2 wherein each resistor string further comprises:

a plurality of resistors coupled in series with one another without any switching resistance between the resistors; and

a respective switch coupled between each node in the resistor string and the second comparison input.

8. The resistance measurement circuit of claim 7 and further comprising:

a control circuit having a plurality of switch control outputs, wherein each switch control output is coupled to a control terminal of a respective one of the switches in each of the resistor strings

and has an input coupled to a comparison output of the comparator.

9. The resistance measurement circuit of claim 8 wherein the control circuit comprises a finite state machine.

10. The resistance measurement circuit of claim 8 and further comprising:

a register block having a plurality of data inputs coupled to the plurality of switch control outputs and a latch control input, which is controlled by the control circuit.

11. The resistance measurement circuit of claim 2 and further comprising a control circuit, which is adapted to wherein the control circuit is adapted to:

sequentially couple successive nodes in a first of the resistor strings in the sequence to the second comparison input until a voltage on a selected one of the nodes in the resistor string causes a comparison output of the comparator to change state; and

sequentially couple the node corresponding to the selected node in each successive one of the resistor strings in the sequence to the second comparison input until the comparison output again changes state.

12. An integrated circuit test structure comprising:

an integrated circuit substrate;

a plurality of current sources on the substrate; and

a plurality of resistor strings on the substrate, wherein each resistor string is coupled in series with a respective one of the current sources and comprises a plurality of nodes with different resistances relative to a reference node, and wherein each node in each resistor string has a different resistance relative to the reference node than corresponding nodes in the other resistor strings.

13. The integrated circuit test structure of claim 12 wherein:

the plurality of resistor strings comprises a sequence of the resistor strings; and

each set of the corresponding nodes in the plurality of resistor strings have progressively varying resistances within the sequence.

14. The resistance measurement circuit of claim 13 wherein:

each node in each resistor string has a smaller resistance relative to the reference node than the corresponding node in the next preceding resistor string in the sequence and a larger resistance relative to the

reference node than the corresponding node in the next succeeding resistor string in the sequence.

15. The resistance measurement circuit of claim 13 wherein:

each resistor string comprises a plurality of resistors coupled in series with one another; and

each resistor string further comprises a least significant one of the resistors, which is coupled to the reference node, and a different number of parallel resistors coupled in parallel with the least significant resistor than are coupled in parallel with the least significant resistors in the other resistor strings.

16. The resistance measurement circuit of claim 13 wherein:

the plurality of resistor strings comprises m+1 resistor strings, which can be indexed in the sequence by a variable i, for i = 0 to m+1, where m is an integer variable;

each resistor string i comprises a plurality of resistors coupled in series with one another, including at least one least significant resistor that is connected to the reference node;

wherein the at least one least significant resistor in resistor string i comprises 2^i resistors coupled in parallel with one another.

17. The resistance measurement circuit of claim 16 wherein each resistor in each resistor string has a unit resistance.

18. The resistance measurement circuit of claim 13 wherein each resistor string further comprises:

a plurality of resistors coupled in series with one another without any switching resistance between the resistors; and

a respective switch coupled between each node in the resistor string and the second comparison input.

19. A method comprising:

(a) passing a bias current through a sequence of resistor strings, wherein each resistor string comprises a plurality of nodes with different resistances relative to a reference node, and wherein each node in each resistor string has a progressively different resistance relative to the reference node than corresponding nodes in preceding resistor strings in the sequence;

(b) sequentially comparing voltages on successive nodes in a first of the resistor

strings to a reference voltage until a voltage on a selected one of the nodes crosses the reference voltage in a first direction; and

(c) after (b), comparing the voltage on the node corresponding to the selected node in successive ones of the resistor strings in the sequence to the reference voltage until the voltage on a selected one of the resistor strings crosses the reference voltage in a second direction, opposite to the first direction.